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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,833	07/25/2001	Jose L. Flores	TNSY:026US/10105470	7148
25094	7590	01/04/2005	EXAMINER	
DLA PIPER RUDNICK GRAY CARY USA, LLP			DOAN, DUC T	
2000 University Avenue			ART UNIT	PAPER NUMBER
E. Palo Alto, CA 94303-2248			2188	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/912,833		FLORES, JOSE L.	
	Examiner		Art Unit	
	Duc T. Doan		2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>08/12/2002 03/24/2</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Status of Claims

1. Claims 1-15 are in the application.

Claims 1-15 are rejected.

Information Disclosure Statement

2. The Information Disclosure Statements received 12 August 2002, 24 March 2003 and 9 February 2004 have been considered. See attached PTO-1449(s).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Magee (US 5729710) in view of Brady (US 5784698).

As for claim 1 and 3, Magee teaches that each application program being executed is called a process (Column 1 line 34). A process comprises of two components called task and thread. A thread is the active execution environment of the process. Thus threads are created by the operating system in order to execute the

Art Unit: 2188

application program (Column 2 lines 62-67). Once a thread is created, the microkernel is invoked to populate the objects of data structures that owned by the thread in memory (Column 4 lines 61-63). Magee further teaches that threads of different processes can gain access to other thread's resource via an unique identifier port number (Column 3 lines 5-34). Threads run simultaneously on distributing processors (Column 1 lines 26-50). Magee further teaches that in a distributing processors system using the threads created by microkernel, thousands of programs can be run concurrently, thus increase the execution throughput of the system (Column 1 lines 31-34). Magee does not describe a structure of memory pools based on size of the memory block nor the procedure of matching size of a memory block into memory pools.

Brady describes an apparatus for dynamically allocating memory includes a processor (Fig 1:#12), a free buffer memory (Fig 1:#14) and a control memory (Fig 1:#18), that stores buffer control block data structures (Fig 2). The control block data structures enable a segmentation of the free buffer memory into a series of free buffer pools. Each free buffer pool comprises plural identical size buffers, each succeeding free buffer pool including a larger buffer size than a preceding free buffer pool. Brady teaches a memory allocation procedure that ^{responds}~~responds~~ to a request from an executing procedure by comparing the request buffer space with the size parameters of free buffer pools. It then allocates a buffer from a free buffer pool in the free buffer pool memory whose selection size parameter is a next larger value among the selection parameter. The comparison is done iteratively until a free buffer is found (Column 2 line 45 to Column 3 line 5). A

Art Unit: 2188

programmable selection size parameter associated with each buffer pool is provided in order to facilitate the buffer pool selection step (Column 5 lines 36-41).

Brady teaches a commonly accepted prior art procedure that is to compare the actual size of the requested buffer space to the buffer size in each free buffer pool. If the size of the needed buffer space is larger than the largest available buffer size in a free buffer pool, then the buffer pool with the largest buffer size is selected. Otherwise, the buffer pool with the buffer size that is just larger than the actual size of the buffer needed is selected (Column 5 lines 14-25).

Brady teaches a sequence of events starting from a request for buffer space issued by an executing procedure to a hardware processor (Fig 1:#12), that carries out the allocation procedure. When the allocation procedure is done, the buffer control block (Fig 2) is passed back to the requestor. Notice that the address of the allocated memory block is a field of the buffer control block (Fig 2).

Brady further teaches that in the prior art procedure, the memory allocation is initiated by a software request and is handled by operating system via interruption (Column 3 lines 20-25). Substantially, all programs require allocation and de-allocation of resources within the system. Brady teaches that s principal objective in carrying out allocation/de-allocation procedures is to minimize their impact on overall system performance (Column 1 lines 13-19).

It would have been obvious to one of ordinary skill in the art at the time of invention to include memory pool data structures and procedures as suggested by Brady in Magee's system to minimizing the impact on the system performance.

As for claim 2, Magee teaches a data paging structure, with pages residing in private cache memory (Fig 6). The segmentation of pages is done by microkernel's virtual memory management (Column 32 lines 1-13). Pages residing in private cache inherently provide faster access to the local processor. By proper managing address spaces of the pages, the microkernel is capable of support large, sparse address spaces, share memory and virtual copy memory optimizations (Column 32 lines 18-24). The page segmentation is done by microkernel's virtual memory management (Column 32 lines 1-13). Pages residing in private cache inherently provide faster access to the local processor. By proper managing address spaces of the pages, the microkernel is capable of support large, sparse address spaces, share memory and virtual copy memory optimizations (Column 32 lines 18-24). Magee does not describe a memory pool data structures. Brady teaches memory pool data structures and an allocate procedure (Column 2 line 45 to Column 3 line 5). It would have been obvious to one of ordinary skill in the art at the time of invention to include data structures and procedures as suggested by Brady in private cache memory of Magee's system to support virtual copy memory optimizations.

As for claim 4, the rationale in the rejection of claim 1 is incorporated herein. Magee does not teach a de-allocation procedure based on size of memory block. Brady teaches a de-allocate procedure using the buffer control block to return the unused memory block to the proper memory pool, and returning the buffer control block to the requestor (Column 4 lines 66-67 and column 5 lines 1-5). In order to return it to the proper memory pool, it must execute the memory pool size-comparing step iteratively.

Art Unit: 2188

Brady teaches that s principal objective in carrying out allocation/de-allocation procedures is to minimize their impact on overall system performance (Column 1 lines 13-19). Using the same rational as in claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention to include de-allocation procedure as suggested by Brady in Magee's system to minimizing the impact on the system performance.

5. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Magee (US 5729710) in view of Brady (US 5784698) as applied to claim 4 above, and further in view of Weldon (US 6275916). Magee does not describe the de-allocation procedure for the memory data structures. Brady teaches a de-allocation procedure (Column 4 lines 66-67 and column 5 lines 1-5). However Brady does not specifically describe different memory spaces to return memory blocks. Weldon describes a de-allocate procedure that uses either the normal heap memory pool or separate memory pool spaces. The selection of appropriate de-allocation memory spaces is done by the regular delete operator or the overloaded operator DELETE (Column 5 and Column 6 lines 1-17). If the de-allocate memory pool is different than the allocate memory pool, the overall availability of the memory pools is improved (Column 1 lines 26-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to include the delete operators as suggested by Weldon and the de-allocation procedure as suggested by Brady in Magee's system to improve the availability of memory pools.

Art Unit: 2188

6. Claim 6-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Magee (US 5729710) in view of Brady (US 5784698) and further in view of Catanzaro (Multi Processor System Architectures).

As for claim 6, the rational in the rejection of claim 1 is incorporated herein.

Magee teaches that threads of different processes in a distribute computing system must use port numbers to communicate with each other. Thus the port numbers allow Brady in Magee's system to the distributing of services over a network without program modification (Column 3 lines 15-23). Magee and Brady do not describe a procedure to search a data structure using a code identify the owning thread. Catanzaro teaches a memory control unit (MMU) of the SPARC processor that runs SOLARIS operating system. The data structures in the MMU are shared by threads that run on SOLARIS. Catanzaro further describes a procedure to search a page table data structure in MMU using the context tag and virtual address tags to identify the owner thread. When the data structure is located, the local physical address that belong to the owning thread is returned to the requesting thread (Pages 93-98). It would have been obvious to one of ordinary skill in the art at the time of invention to include the context tag and virtual address tag as suggested by Catanzaro, data structures and procedures as suggested by Brady in Magee's system to allows the distributing of services over a network without program modification.

As for claim 7, Magee teaches that resources are shares among threads (Column 3 lines 8-10). Thus threads can execute a program concurrently (Column 3 lines 3-6). Magee and Brady do not limit the memory spaces in which the data

Art Unit: 2188

structures reside. Catanzaro teaches a page table data structure that resides in a shared memory spaces in the MMU unit (Pages 93-98). It would have been obvious to one of ordinary skill in the art at the time of invention to apply the data structure that resides in a shared memory as suggested by Catanzaro, memory pools data structures and procedures as suggested by Brady in Magee's system to allow threads execute a program concurrently.

As for claim 8, the rational in the rejection of claim 1 is incorporated herein. Magee teaches a data paging structure, with pages residing in private cache memory (Fig 6). The page segmentation is done by microkernel's virtual memory management (Column 32 lines 1-13). Pages residing in private cache inherently provide faster access to the local processor. By proper managing address spaces of the pages, the microkernel is capable of support large, sparse address spaces, share memory and virtual copy memory optimizations (Column 32 lines 18-24).

Magee and Brady do not limit the memory type in which the memory pool data structures are used. Catanzaro describes a processor with private memory (Fig 3-3 page 55). It would have been obvious to one of ordinary skill in the art at the time of invention to apply the private memory as suggested by Catanzaro, memory pool data structures and procedures as suggested by Brady in Magee's system and virtual copy memory optimizations.

As for claim 9, Magee and Brady do not limit the processor's technology in which the buffer control block is implemented. Catanzaro teaches a low-cost microprocessor designed by LSI LOGIC for use in the desktop SPARC workstation (page 54-55). It

Art Unit: 2188

would have been obvious to one of ordinary skill in the art at the time of invention to apply the microprocessor suggested by Catanzaro, memory pool data structures and procedures as suggested by Brady in Magee's system to allow for an economic implementation of a processor.

As for claim 10, Magee and Brady do not limit the processor configuration in which the memory pool data structures are implemented. Catanzaro teaches a processor SPARC SERVER 1000 designed by SUN MICROSYSTEMS providing two independent processor modules (Fig 9-17, page 300-301). It would have been obvious to one of ordinary skill in the art at the time of invention to apply the microprocessor as suggested by Catanzaro, memory pool data structures and procedures as suggested by Brady in Magee's system to allow concurrent execution of processes.

As for claims 11-13, Magee teaches using the share memory to optimize and support large virtual address spaces (Column 9 lines 40-45, column 10 lines 1-15). Magee and Brady do not limit the processor configurations and memory spaces in which the memory pools are used. Catanzaro teaches a shared memory space capable of being accessed by two processor modules. And data structures in private cache are backed up with copies in main memory (Fig 9-17, page 300-301). It would have been obvious to one of ordinary skill in the art at the time of invention to apply the shared memory subsystem as suggested by Catanzaro in Magee's system to optimize large virtual address space.

As for claim 14-15, Brady teaches a memory pool data structures, which comprises of buffer control blocks implemented as a link list data structure (Fig 2).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Benayon (US 6816956). User control of multiple memory heaps. Benayon describes a system in which the request for memory blocks is handled by an application program and the runtime library component of operating system only.

Bonola (Pub US 20010011338). System method and apparatus for providing linearly scalable dynamic memory management in a multiprocessing system. Bonola describes a system with allocation and de-allocation procedures. It compares the request block size to all contiguous sub block sizes using addresses sorted by power of 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2188

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
7/24/04

DD

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SUPERVISORY PATENT EXAMINER